Program Correction

Oct. 4, 2013

Canceled papers:

Mo-P-22

Defect Characterization on SiC Substrates for Room-Temperature Single Photon Source

J. Sun[1)], Y. Satoh[1)], T. Umeda[1)], B. C. Johnson[2)], T. Makino[2)], S. Onoda[2)], and T. Ohshima[2)]
[1)]University of Tsukuba, Japan, [2)]Japan Atomic Energy Agency, Japan

Tu-P-37

Die Attach for High Temperature Applications

J. -F. Barbot and A. Drevin-Bazin
Université de Poitiers, France

We-P-47

Breakdown Voltage Enhancement in 4H-SiC Schottky Diode Employing Field Plate Edge Termination Using High-k Dielectrics

B. Shankar[1,2)], S. K. Gupta[1)], W. R. Taube[1)], J. Singh[1)], A. Asati[2)], and J. Akhtar[1)]
[1)]CSIR-Central Electronics Engineering Research Institute, India, [2)]Birla Institute of Technology and Science, India

We-P-53

HVPE for the Growth of UV LED Heterostructures

S. Y. Kurin[1)], A. A. Antipov[1)], I. S. Barash[1)], A. D. Roenkov[1)], H. I. Helava[2)], B. P. Papchenko[3)], and Y. N. Makarov[2)]
[1)]Nitride Crystals Ltd., Russia, [2)]Nitride Crystals Inc., USA, [3)]University ITMO, Russia

Th-1A-1 <Invited>

Threshold-Voltage Stability: Key Reliability Issue for SiC Power MOSFETs

A. Lelis, R. Green, D. Habersat, and M. El
U.S. Army Research Laboratory, USA

Th-3A-5 <Late News>

High Quality and High Speed Cutting of 4H-SiC JFET Wafers Including PCM Structures by Using Thermal Laser Separation

D. Lewke[1)], M. Koitzsch[1)], K. O. Dohnke[2)], M. Schellenberger[1)], H. -U. Zühlke[3)], L. Pfitzner[1)], and H. Ryssel[1)]
[1)]Fraunhofer Institute for Integrated Systems and Device Technology IISB, Germany, [2)]Infineon Technologies AG, Germany, [3)]JENOPTIK Automatisierungstechnik GmbH, Germany

Th-P-15

Optical and Surface Science Studies of 3C-SiC on Si Grown by Chemical Vapor Deposition

D. Xie[1)], Y. T. He[2)], T. Mei[1)], Z. R. Qiu[2)], and Z. C. Feng[3)]
[1)]South China Normal University, China, [2)]Sun Yat-Sen University, China, [3)]National Taiwan University, Taiwan

(Posters not put on the poster board were regarded as canceled.)

Author corrected paper:

Th-P-62

Characterization of 4H-SiC Homoepitaxial Layers Grown on 100-mm-Diameter 4H-SiC/Poly-SiC Bonded Substrates

J. Suda[1)], T. Okuda[1)], H. Uchida[2)], A. Minami[2)], N. Hatta[2)], T. Sakata[2)], T. Kawahara[2)], K. Yagi[2)], Y. Kurashima[3)], and H. Takagi[3)]

[1)]Kyoto University, Japan, [2)]SICOXS Co., Japan, [3)]National Institute of Advanced Industrial Science and Technology, Japan

Plenary lecture fixed:

Fr-PL-1 <Invited>

High Speed Rail Awaits the Next Breakthrough of Power Semiconductors

T. Uzuka and E. Masada

Railway Technical Research Institute, Japan

Session Chairpersons

Tu-1A High Voltage Devices 1 8:30-10:20

Chairs: Y. Yonezawa (AIST, Japan)

R.Singh (GeneSiC Semiconductor, USA)

Th-2B MOS Fundamentals 10:40-12:30

Chairs: T. Hatakeyama (AIST, Japan)

K. Fukuda (AIST, Japan)